IN THE CLAIMS

1. (Previously Presented) A printed circuit board comprising:

a first conductive plane;

a second conductive plane substantially parallel to the first conductive plane;

a via signal barrel transecting the first and second conductive planes;

a first anti-pad positioned between the first conductive plane and the via signal barrel, the first anti-pad having a first voided area and a first non-voided area; and

a second anti-pad positioned between the second conductive plane and the via signal barrel, the second anti-pad having a second voided area and a second non-voided area;

wherein the first voided area does not completely overlap the second voided area.

2. (Original) The printed circuit board of claim 1, wherein the first conductive plane comprises one of a power plane and a ground plane.

3. (Original) The printed circuit board of claim 1, wherein the second conductive plane comprises one of a power plane and a ground plane.

4. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are longer in a first direction than in a second direction.

5. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are partially voided anti-pads.

6. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are configured to maintain board planarity.

7. (Original) The printed circuit board of claim 1, wherein the first and second anti-pads are configured for signals through the via signal barrel greater than approximately 2 GHz.

8. (Original) A printed circuit board comprising:

a first conductive plane;

a second conductive plane substantially parallel to the first conductive plane;

a via signal barrel transecting the first and second conductive planes;

a first partially voided anti-pad positioned between the first conductive plane and the via signal barrel, the first partially voided anti-pad having a first pattern and a first orientation; and

a second partially voided anti-pad positioned between the second conductive plane and the via signal barrel, the second partially voided anti-pad having a second pattern and a second orientation;

wherein the first orientation is offset from the second orientation.

9. (Original) The printed circuit board of claim 8, wherein the first and second partially voided anti-pads are configured to maintain planarity of the printed circuit board.

10. (Original) The printed circuit board of claim 8, wherein the first and second patterns are substantially identical.

11. (Original) The printed circuit board of claim 8, wherein the first and second partially voided anti-pads are configured for signals through the via signal barrel greater than approximately 2 GHz.

12. (Original) The printed circuit board of claim 8, wherein the first pattern comprises one of a symmetric pattern and an asymmetric pattern.

13. (Original) The printed circuit board of claim 8, wherein the first pattern comprises one of a concentric circles pattern, a radial spokes pattern, and an arbitrary pattern.

14. (Original) The printed circuit board of claim 8, wherein the first pattern comprises a screen pattern.

15. (Original) A printed circuit board comprising:

a first conductive plane;

a second conductive plane substantially parallel to the first conductive plane;

a first via signal barrel transecting the first and second conductive planes;

a first anti-pad positioned between the first conductive plane and the first via signal barrel, the first anti-pad having a first length and a first width and a first orientation; and

a second anti-pad positioned between the second conductive plane and the first via signal barrel, the second anti-pad having a second length and a second width and a second orientation;

wherein the first orientation is offset from the second orientation.

16. (Original) The printed circuit board of claim 15, wherein the first length and the first width are not equal.

17. (Original) The printed circuit board of claim 15, wherein the second length and the second width are not equal.

18. (Original) The printed circuit board of claim 15, wherein the first and second anti-pads are configured to maintain planarity of the printed circuit board.

19. (Original) The printed circuit board of claim 15, wherein the first and second anti-pads are configured for signals through the first via signal barrel greater than approximately 2 GHz.

20. (Original) The printed circuit board of claim 15, wherein the first length substantially equals the second length and the first width equals the second width.

21. (Original) The printed circuit board of claim 15, wherein the first and second anti-pads are substantially oval shaped.

22. (Original) The printed circuit board of claim 15, wherein the first orientation is substantially perpendicular to the second orientation.

23. (Original) The printed circuit board of claim 15, further comprising:

a second via signal barrel parallel to the first via signal barrel and transecting the first and second conductive planes;

a third anti-pad positioned between the second via signal barrel and the first conductive plane, the third anti-pad having a third orientation; and

a fourth anti-pad positioned between the second via signal barrel and the second conductive plane, the fourth anti-pad having a fourth orientation;

wherein the first and third orientations are substantially identical and adapted to allow a signal trace between the first and third anti-pads on an adjacent signal plane.

24. (Original) A method for forming a printed circuit board, comprising:

providing a first conductive plane;

providing a second conductive plane substantially parallel to the first conductive plane;

forming a via signal barrel transecting the first and second conductive planes;

forming a first anti-pad positioned between the first conductive plane and the via signal barrel, such that the first anti-pad has a first orientation and a first void; and

forming a second anti-pad positioned between the second conductive plane and the via signal barrel, such that the second anti-pad has a second orientation and a second void;

wherein the first orientation is offset from the second orientation; and

wherein the first void does not completely overlap the second void.

25. (Original) The method of claim 24, wherein the first and second anti-pads are configured to maintain planarity of the printed circuit board.

26. (Original) The method of claim 24, wherein the first and second anti-pads are substantially oval shaped.

27. (Original) The method of claim 24, wherein the first and second anti-pads are partially voided in a pattern.

28. (Original) The method of claim 27, wherein the pattern comprises one of a symmetric pattern and an asymmetric pattern.

29. (Original) The method of claim 27, wherein the pattern comprises one of a concentric circles pattern, a radial spokes pattern, and an arbitrary pattern.

30. (Original) The method of claim 27, wherein the pattern comprises a screen pattern.

31. (Original) The method of claim 24, wherein the first and second anti-pads are configured for signals through the via signal barrel greater than approximately 2 GHz.